

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory ,CPU-PEG/Display	3,4
05 CPU-Control/MISC/CFG/Audio	5
CPU-Power/CPU-GND	6,7
DDR 4 DIMM1 & DDR 4 DIMM2	8,9
DDR4-POWER/GND-1 &DDR4-POWER/GND-2	10,11
PCH-USB/PCIE/DMI /SATA	12
PCH-Audio/Display/Clock	13
PCH-GPIO/USB0C#/SATASTRAP	14
PCH-LPC/SPI/SMBUS/MISC	15
PCH-Power,PCH-GND,PCH-Strap	16,17,18
PCIE SLOT-CPU(X16),PCIE SLOT-PCH(X1)	19,20
ASM1142 USB3.1 Host/NA	21,22
BIOS ROM/TPM/Debug LED	23
AUDIO 887, AUDIO de-pop circuit	24,25
LAN - Intel I219V	26
DVI,HDMI,VGA Connector	27,28,29
USB2.0 & USB3.0 & SATA Connector	30,31,32
SIO-NCT6793D,CLR COMS&CUT VBAT	33,34,35
CPU FAN & SYS FAN Controllor	36,37
ATX F_Panel/EMI/ECO/ACPI Controller UPI	38,39
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	40,41,42
DDR-RT8231 & DDR-MP2147-VPP25	43,44
VCCSA POWR-UP1540Q/VCCIO POWER-NB681	45,46
VCCSTPLL/PCH Core power_RT8125	47,48
NA/Manual parts	49,50
Power Map/Power Sequence/GPIO MAP	51,52,53
Revision History	54

# MS-7994

mATX  
Ver: 10(206x243)

## Intel -Skylake plamform

### CPU:

SKL-S LGA1151  
CPU POWER PAK \*3 Phase  
GT POWER PAK \*2 Phase

### Onboard Chip:

HD Audio Codec:ALC887  
LAN-Intel I219V  
SIO:Nuvoton 6793D  
Flash ROM: SPI 64MB  
DP to VGA: ITE6515  
ASM1142 USB3.1 Host

### Main Memory:

DDR4 \*2

### Expansion Slots:

PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 2  
PCI Slot \* 1

### Other:

SATA3.0 x4(PCH)  
SATA Express x1(PCH)  
REAL USB2.0 \*2  
REAL USB3.0 \*4  
FRONT USB2.0 \*4  
FRONT USB3.0 \*2

### System Chipset:

SPT-H B150

### PWM:

VCORE PWM-RT3606  
DDR -RT8231  
PCH(1.0V) -RT8125E  
VCCSA - UP1540Q  
VCCIO - NB681(Converter)

### ACPI:

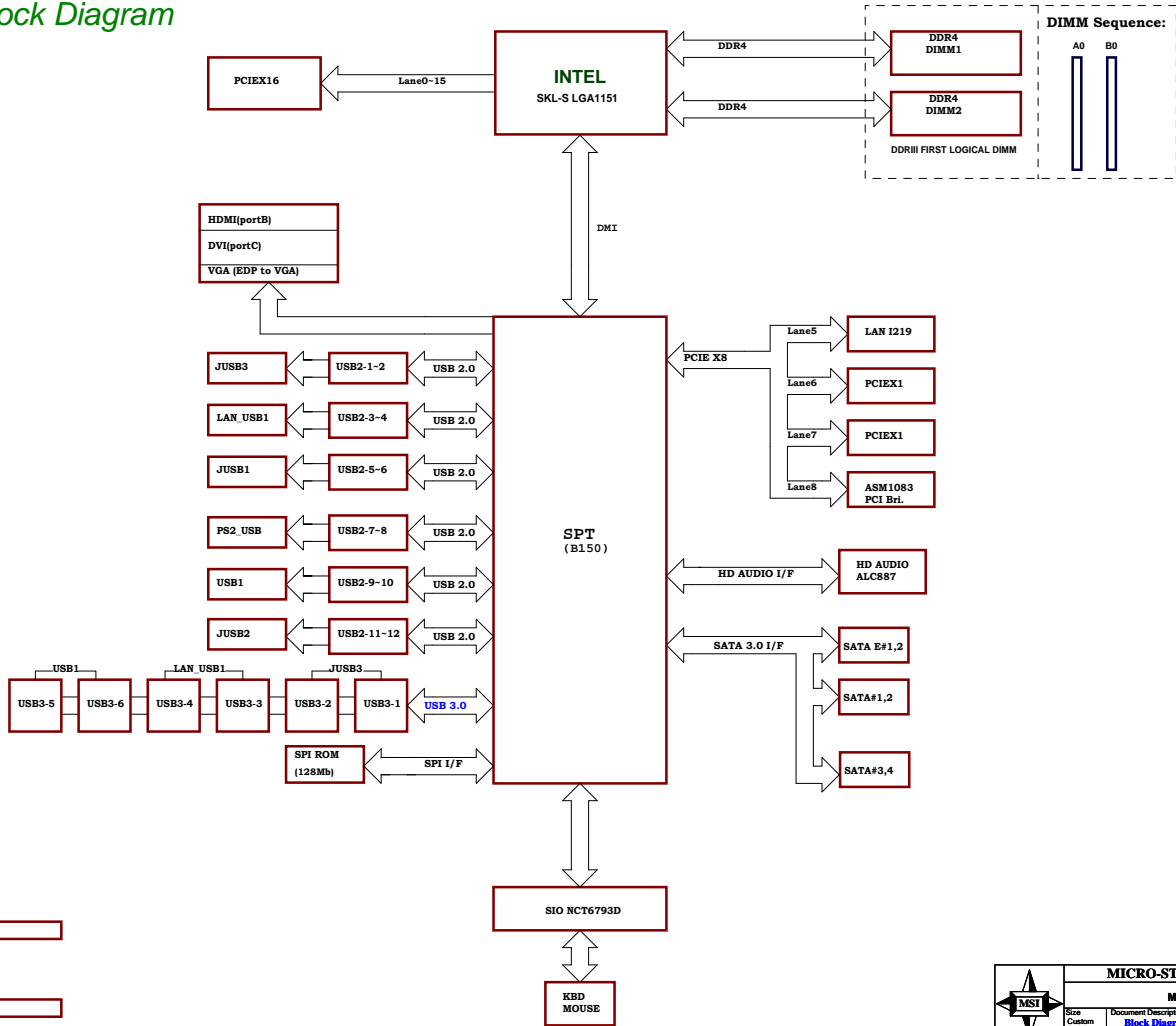
5VDAUL:uP7501  
5VDIMM:uP7501  
3VSB:GS7166+N MOS  
3VDSW:GS7166

### LDO:

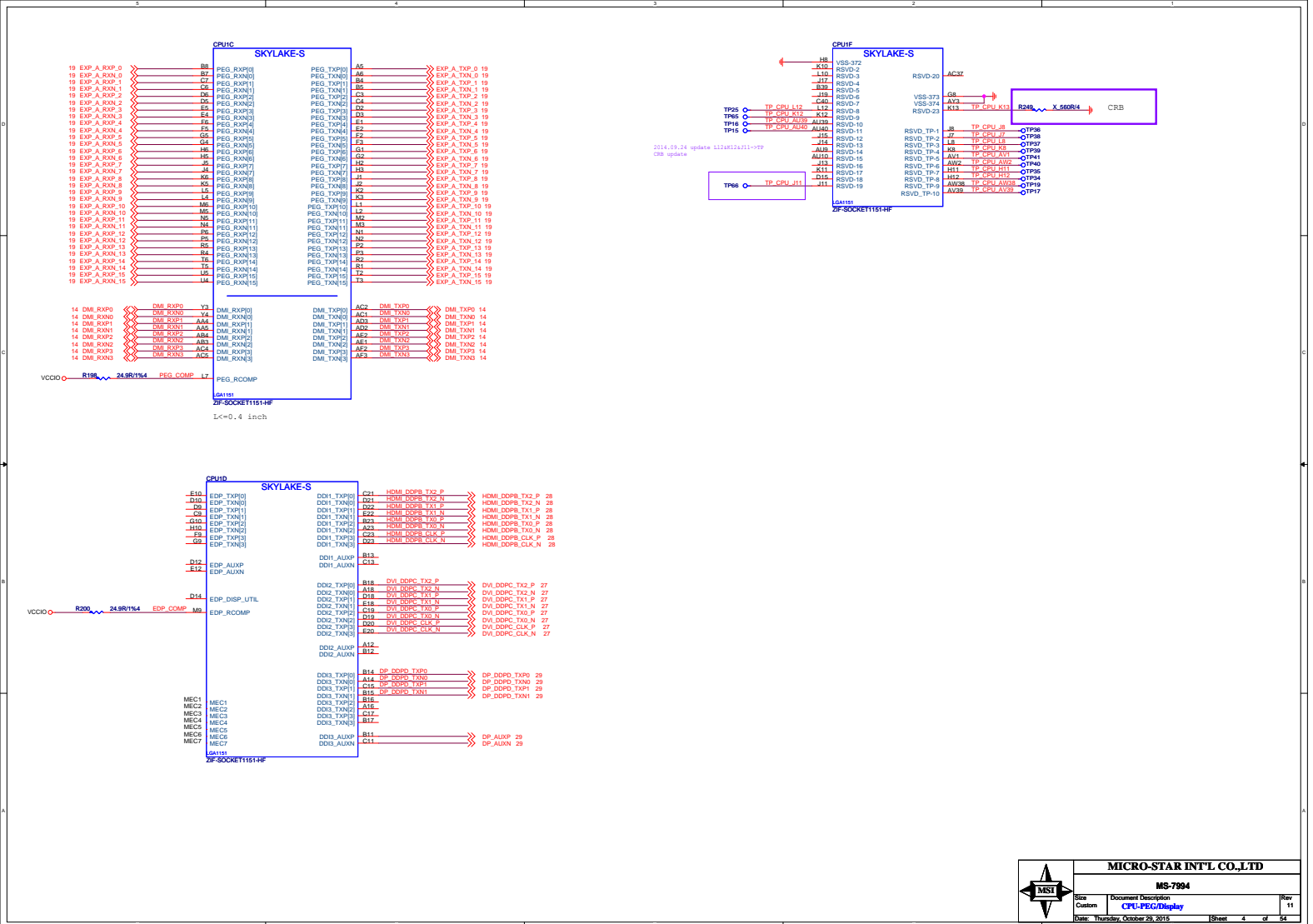
VCCSTPLL - GS7166

MICRO-STAR INT'L CO.,LTD		
MS-7994		
Doc Custom	Document Description Cover Sheet	Rev 11
Date: Thursday, October 28, 2015		Sheet 1 of 54

MS-7994 Block Diagram

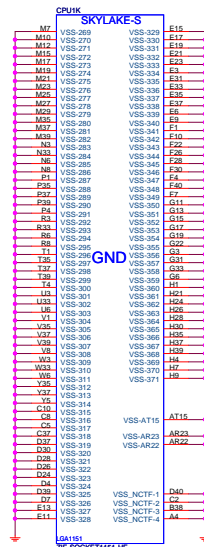
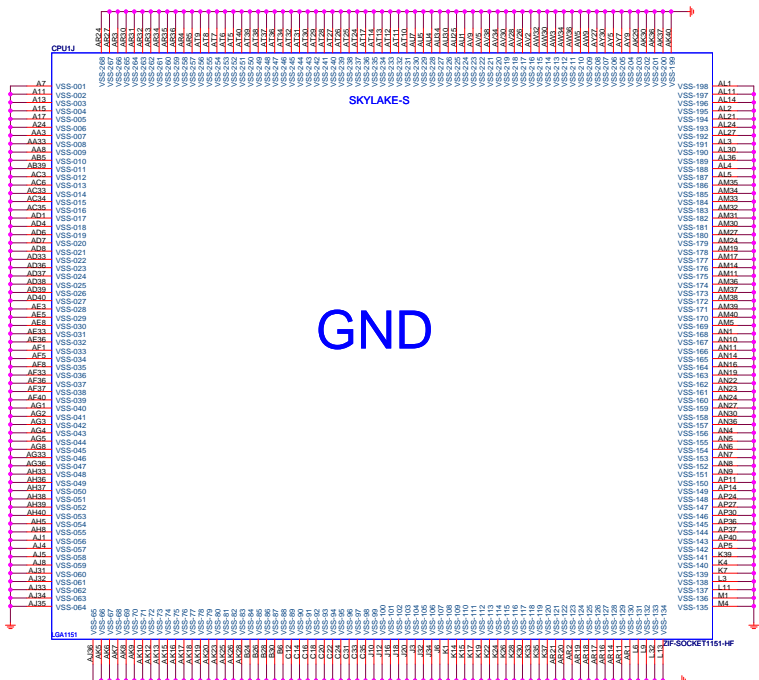


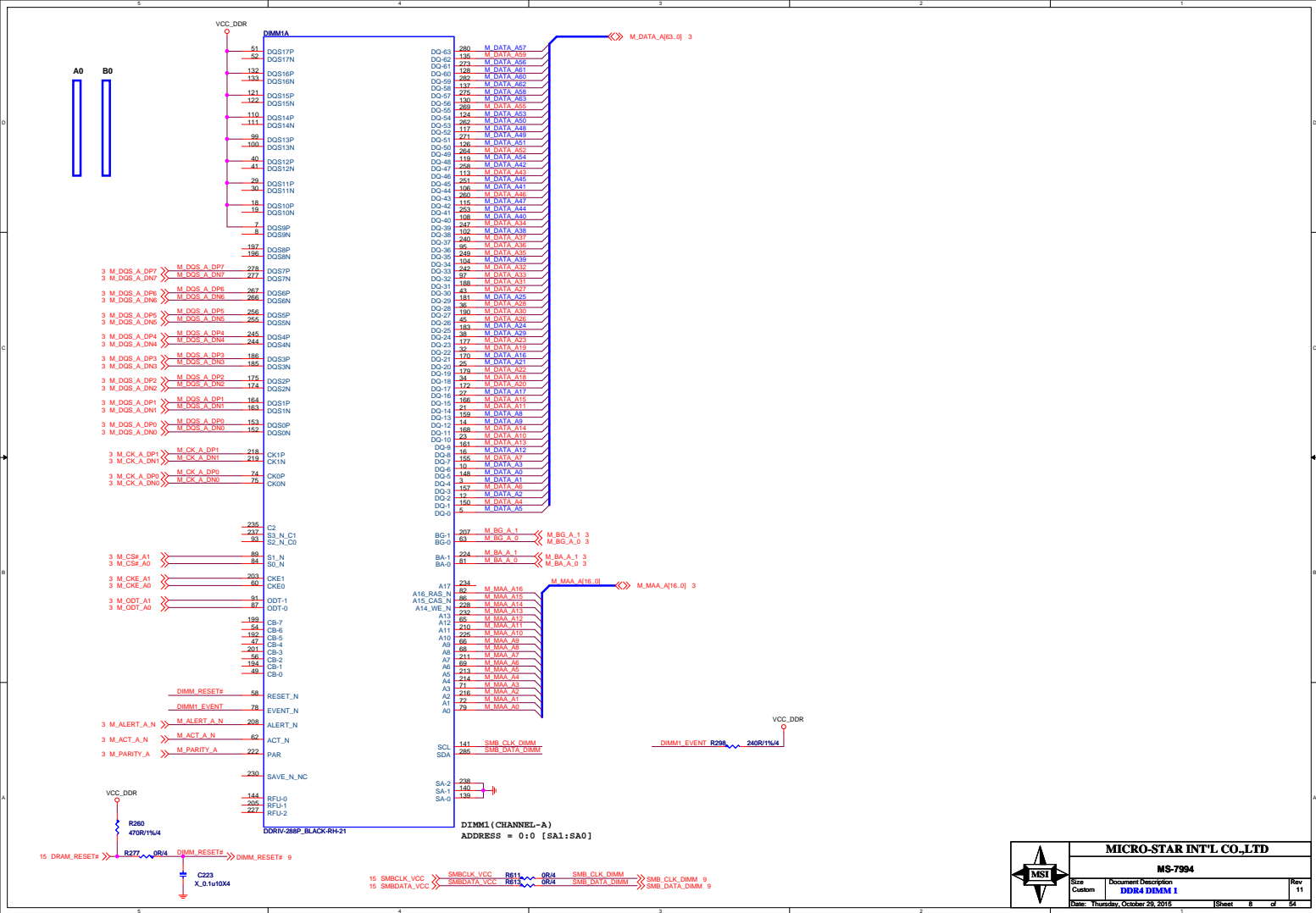




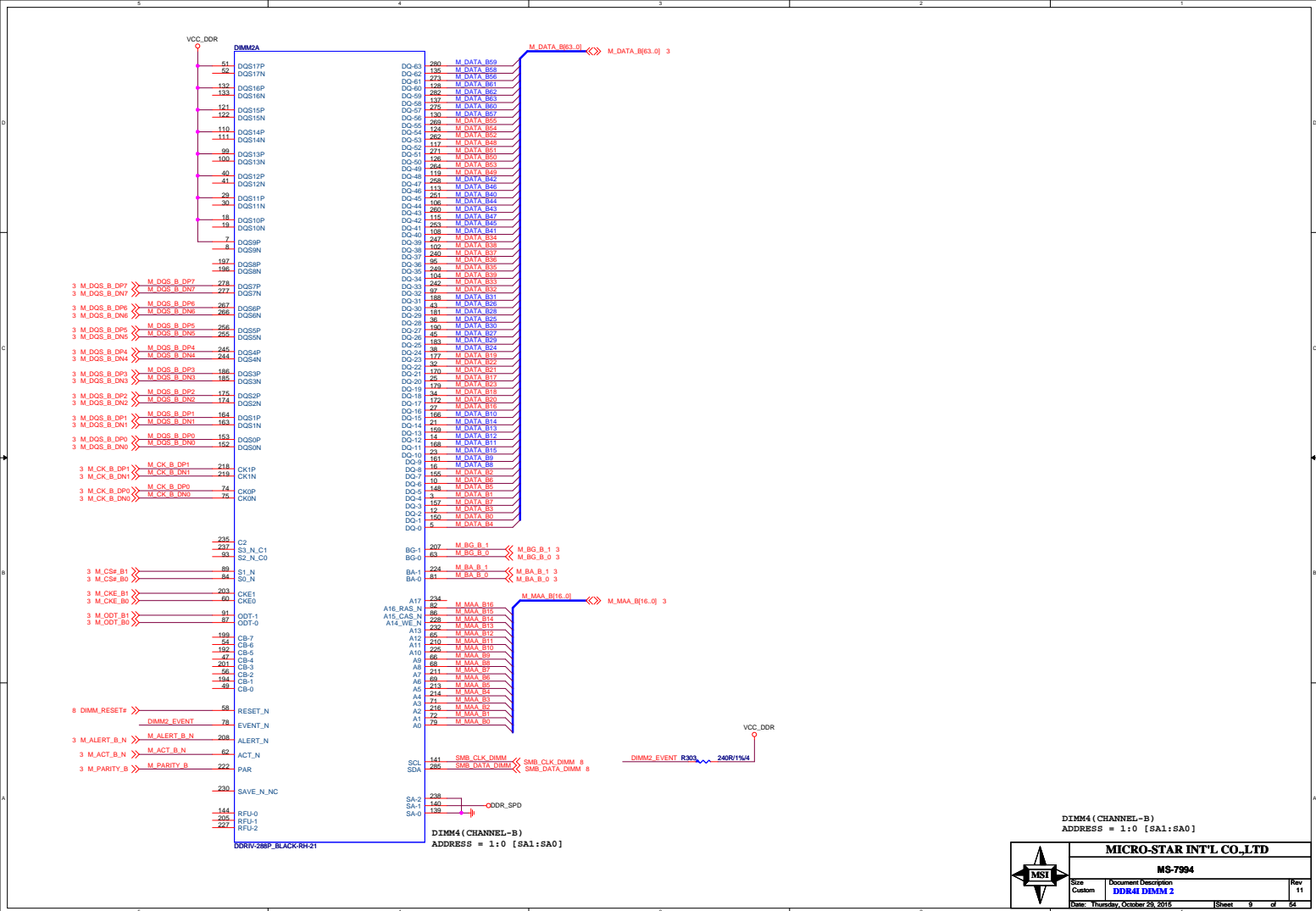


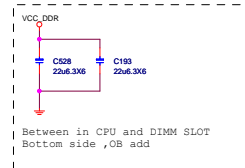
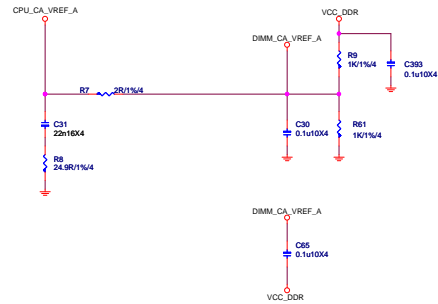
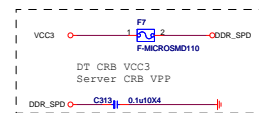
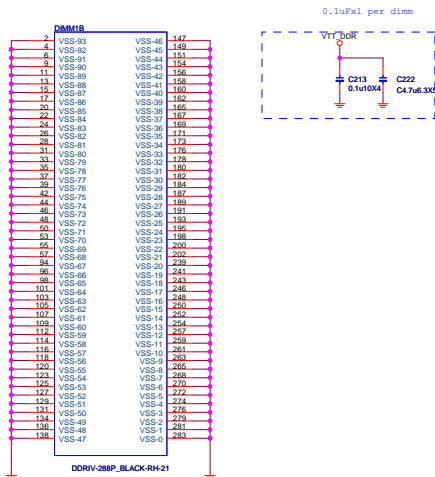
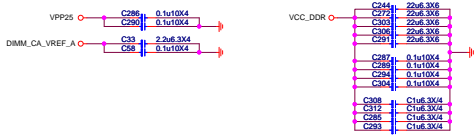
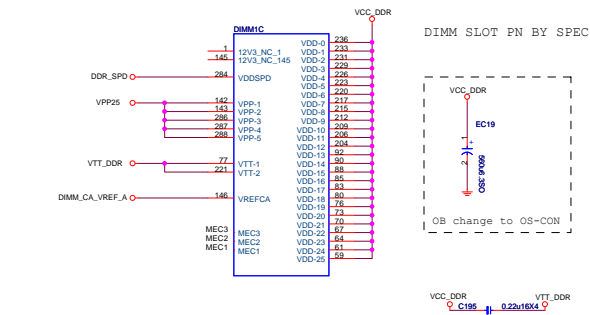






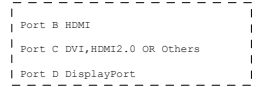




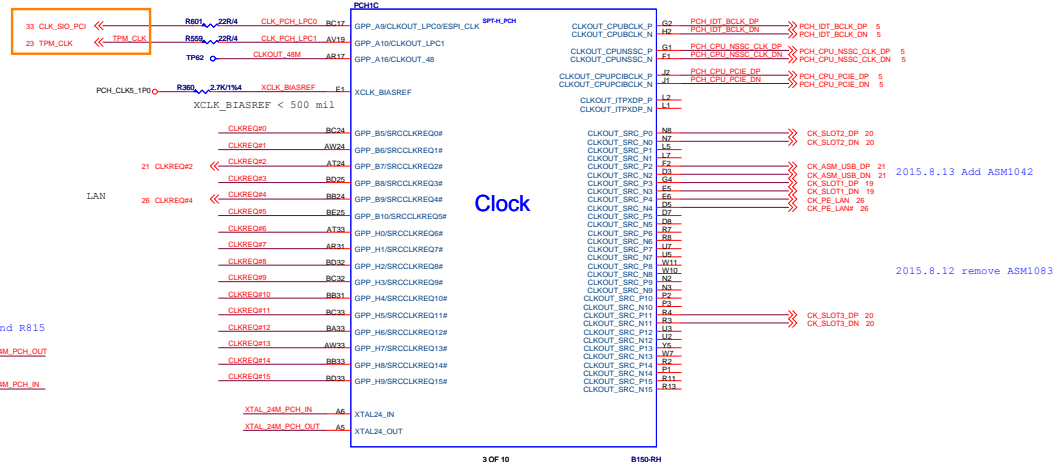


MICRO-STAR INT'L CO.,LTD			
MS-7994			
Size	Document Description	Rev	
Custom	DDR4-POWER/GND-1	11	
Date: Thursday, October 26, 2018		Sheet 10 of 54	

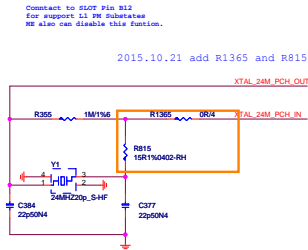




2015.8.14 remove CLOCK BUFFER

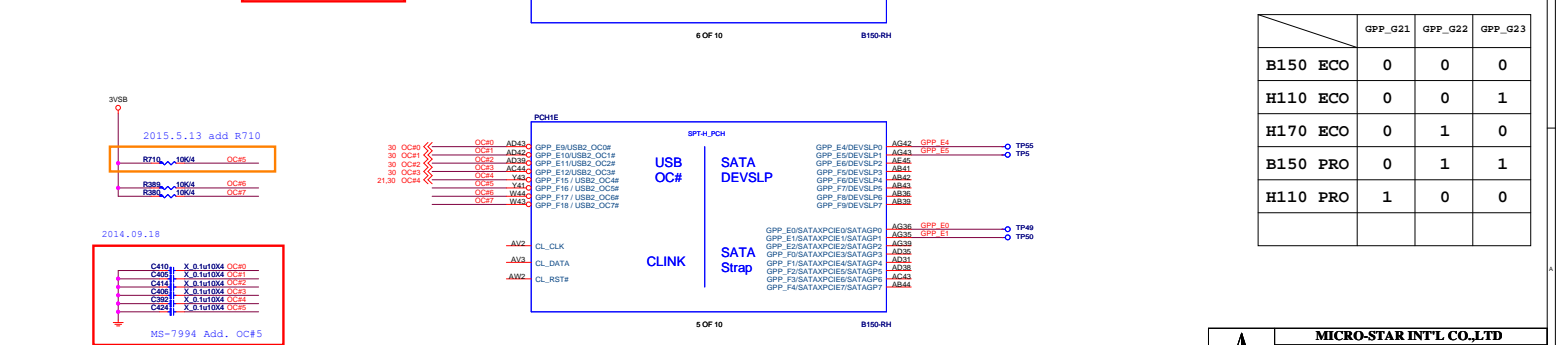
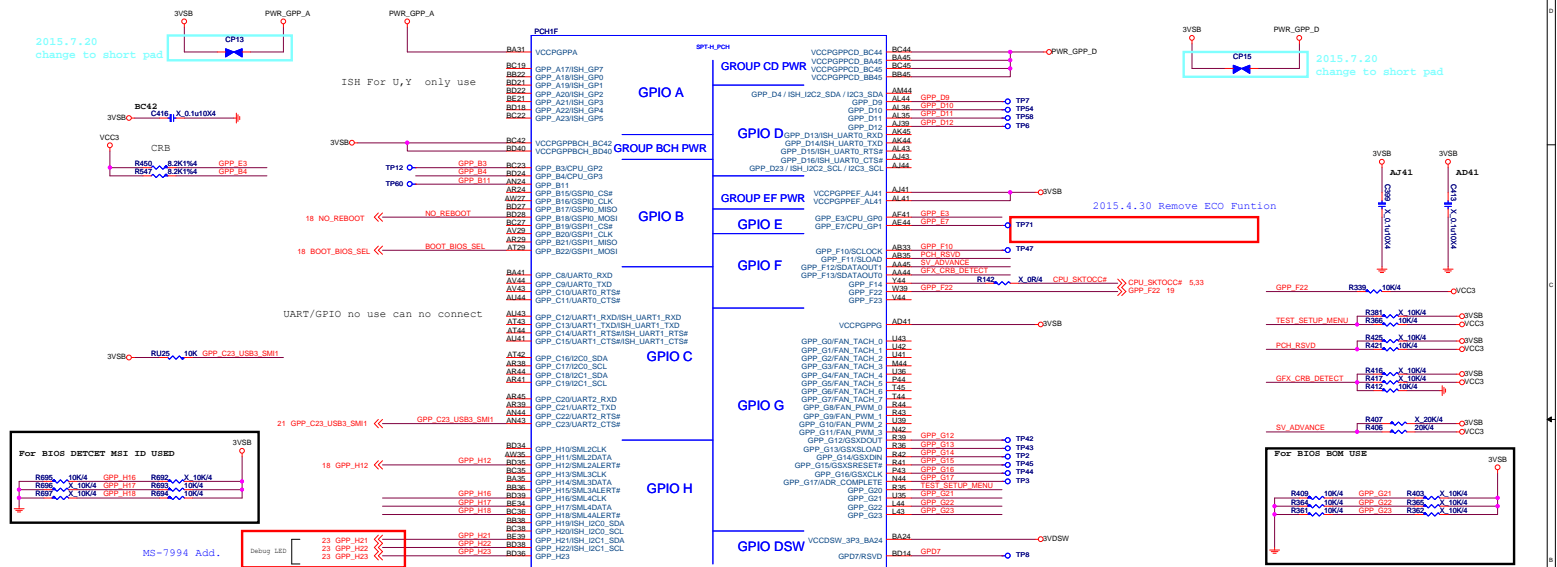


2015.8.12 remove ASM1083 PCI



2015.7.20  
change to short pad

2015.7.20  
change to short pad



MICRO-STAR INT'L CO.,LTD			
MS-7994			
Size	Document Description	Rev	11
Custom	PCB-GPP/USB/OC#SATASTRAP		
Date: Thursday, October 29, 2015	Sheet 13	of	54

H110:1-4  
B150:1-6

H110:1-10  
B150:1-12

PC11A

SPT4\_PCH

USB 3.0

USB 2.0

PCIe/USB 3

PCIe

DMI

H110:N/A  
B150:N/A

H110:N/A  
B150:N/A

PCIECOMP\_P  
PCIECOMP\_N Length Match < 5mll

1 OF 12

B150-RH

PC11B

SPT4\_PCH

PCIe/SATA

H110:N/A  
B150:2

H110:N/A  
B150:2

GPP\_EBSATALEDN AD44 PCH\_SATA\_LEDN# 38

2 OF 10

B150-RH

R429

10K14

Q/CC3

USB2\_COMP  
USB2\_VBUSSENSE  
USB2\_ID

DM1\_TXP0  
DM1\_TXN0  
DM1\_TXP1  
DM1\_TXN1  
DM1\_TXP2  
DM1\_TXN2  
DM1\_TXP3  
DM1\_TXN3

DM1\_RXP0  
DM1\_RXN0  
DM1\_RXP1  
DM1\_RXN1  
DM1\_RXP2  
DM1\_RXN2  
DM1\_RXP3  
DM1\_RXN3

1 OF 12

B150-RH

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/10G	USB3/10G	USB3/10G	USB3/10G	N/A	N/A	N/A	N/A	N/A	LAN Only	LAN	PCIe	PCIe	PCIe
B150	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	N/A	N/A	N/A	N/A	LAN Only	LAN	PCIe	PCIe	PCIe
H170	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
B170	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	USB3/10G	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe

SKU	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/LAN	PCIe	N/A	LAN	SATA*/SATA*	SATA	SATA	N/A	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN	PCIe	N/A	LAN	SATA*/SATA*	SATA	SATA	N/A	N/A	N/A	N/A	N/A	0
H170	PCIe/LAN	PCIe	LAN	LAN	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	2
B170	PCIe/LAN	PCIe	LAN	LAN	SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	2

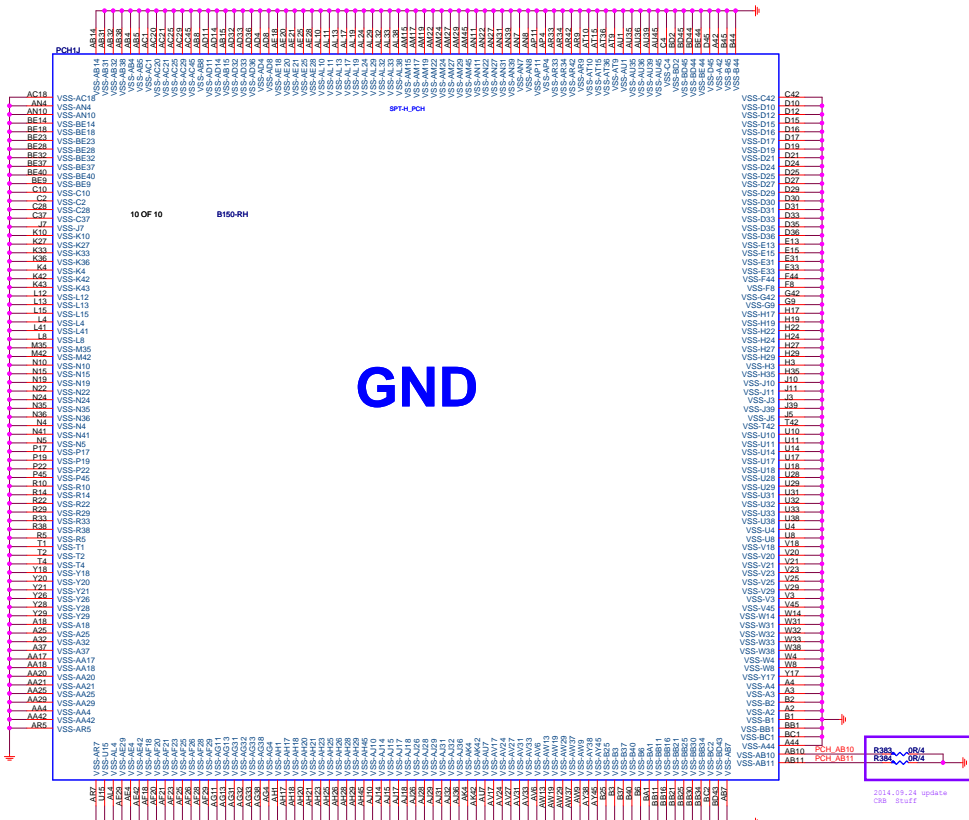


MICRO-STAR INT'L CO.,LTD	
MS-7994	
Doc	Document Description
Custom	PCB-USB/PCIe/DMI/SATA
Date: Thursday, October 29, 2015	Sheet 14 of 54



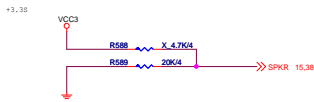






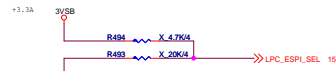
MICRO-STAR INT'L CO.,LTD		
MS-7994		
Size	Document Description	Rev
Custom	PCB-GND	11
Date: Thursday, October 29, 2015		Sheet 17 of 54

TOP Swap



Internal pull-down is disabled after PLTRST#

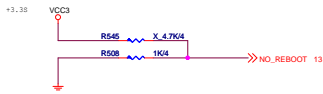
LPC eSPI Mode



0 : LPC  
1 : eSPI

Internal pull-down is disabled after RSMRST

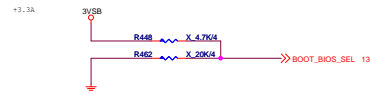
No Reboot



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down is disabled after PLTRST#

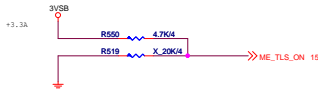
Boot BIOS



0 : SPI  
1 : LPC

Internal pull-down is disabled after PLTRST

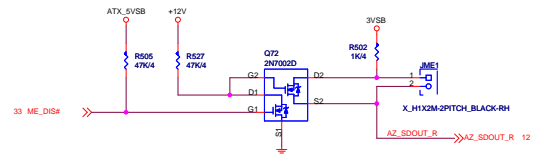
AMT and SBA with confidentiality



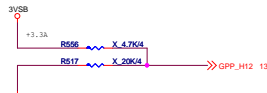
0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA\_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

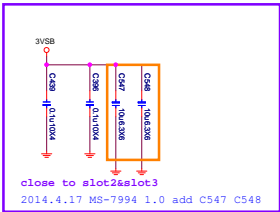
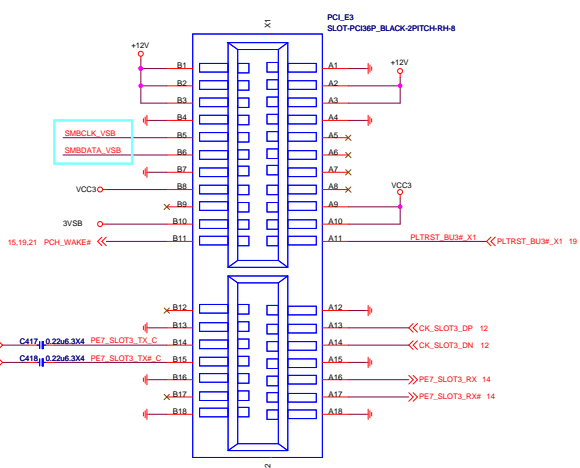
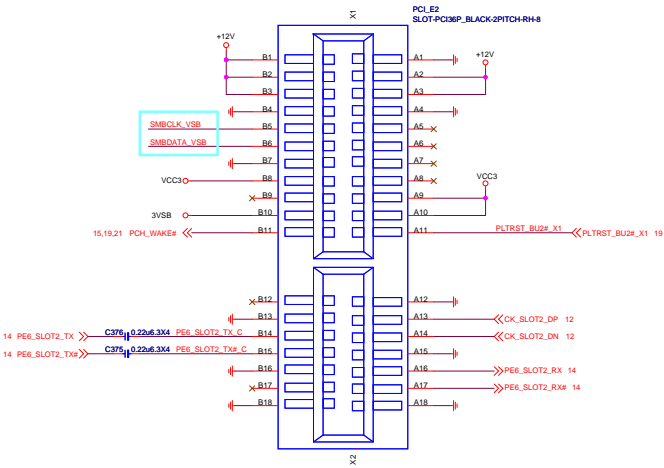
Internal pull-down is disabled after RSMRST

<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7994</b>		
Size	Document Description	Rev
Custom	<b>PCH-Strap</b>	11
Date: Thursday, October 29, 2015		Sheet 18 of 54



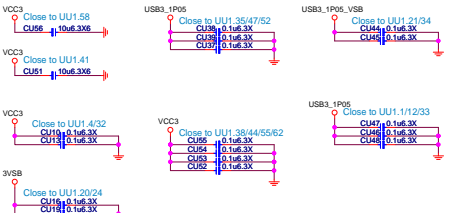
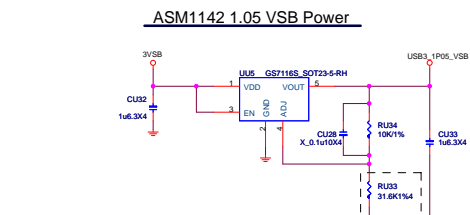
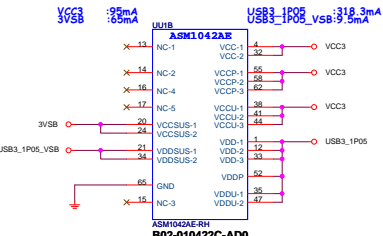
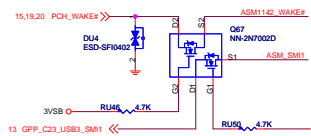
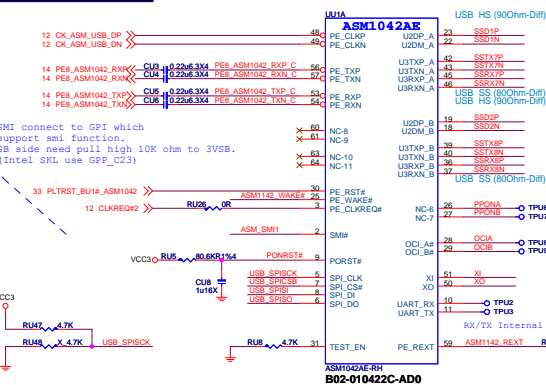
2015.7.20  
change net name to SMBCLK\_VSB,SMBDATA\_VSB

15,19,43 SMBCLK_VSB	>>	SMBCLK_VSB
15,19,43 SMBDATA_VSB	>>	SMBDATA_VSB

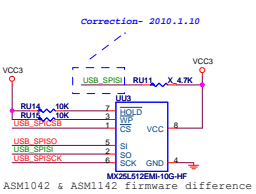


MICRO-STAR INT'L CO.,LTD		
MS-7994		
Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	11
Date: Thursday, October 29, 2015		Sheet 20 of 54

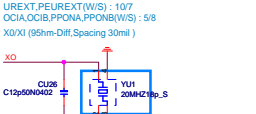
## ASM1042 USB3.0



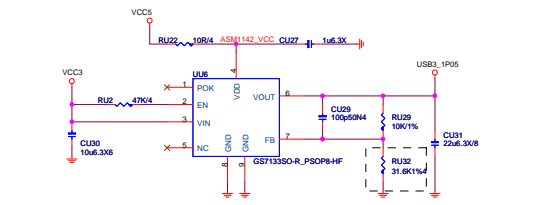
## EEPROM



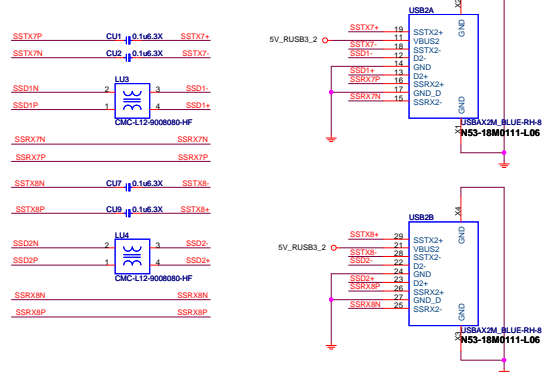
Layout Guide:  
1.) USB3.1 to Connector Total Length < 1.5"  
2.) VIA hole < 2



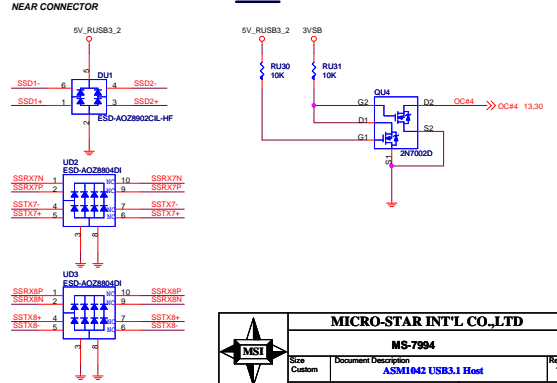
## ASM1042 1.05 Power



## Rear USB3 CONN



## ESD Protection



MICRO-STAR INT'L CO.,LTD			
MS-7994			
Size	Document Description	Rev	11
Custom	ASM1042 USB3.1 Host		
Date: Thursday, October 28, 2016	Sheet	21	of 54

5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

MSI

Size

Custom

Document Description


NA

Date: Thursday, October 29, 2015

Sheet 22 of 54

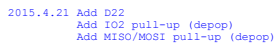
MS-7994

Rev 11



MICRO-STAR INT'L CO.,LTD		
MS-7994		
Size	Document Description	Rev
Custom	NA	11
Date: Thursday, October 26, 2018		Sheet 22 of 54

15	PCH_SPI_MOSI	↔	PCH_SPI_MOSI
15	PCH_SPI_MISO	↔	PCH_SPI_MISO
15	PCH_SPI_CLK	↔	PCH_SPI_CLK
15	PCH_SPI_CS0#	↔	PCH_SPI_CS0#
15	PCH_SPI_I02	↔	PCH_SPI_I02
15	PCH_SPI_I03	↔	PCH_SPI_I03



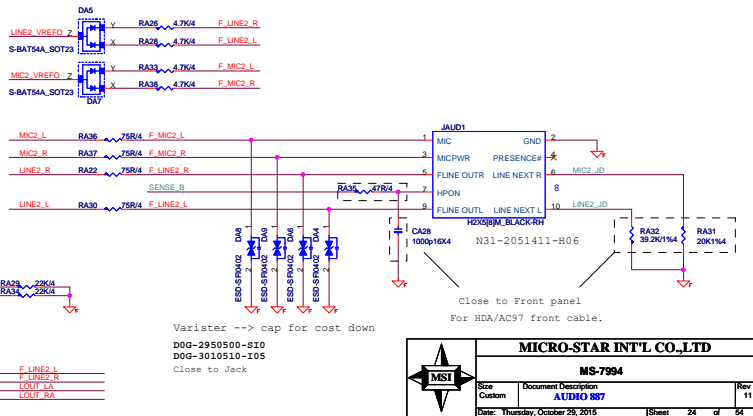
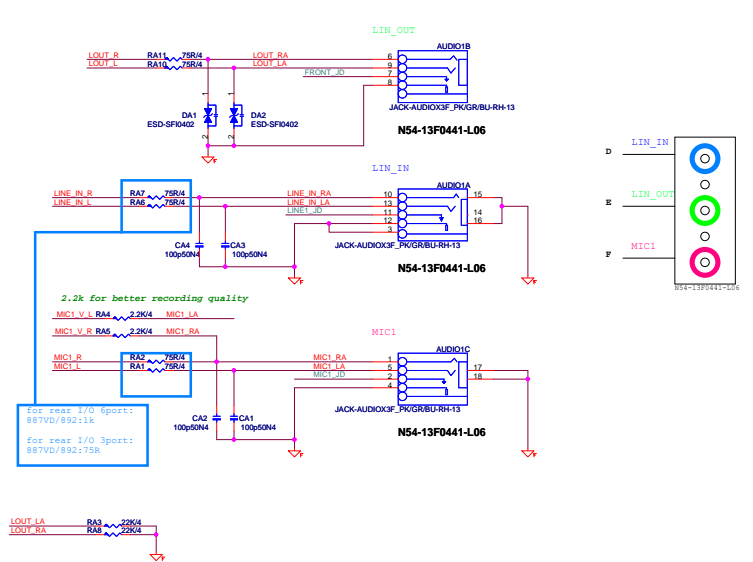
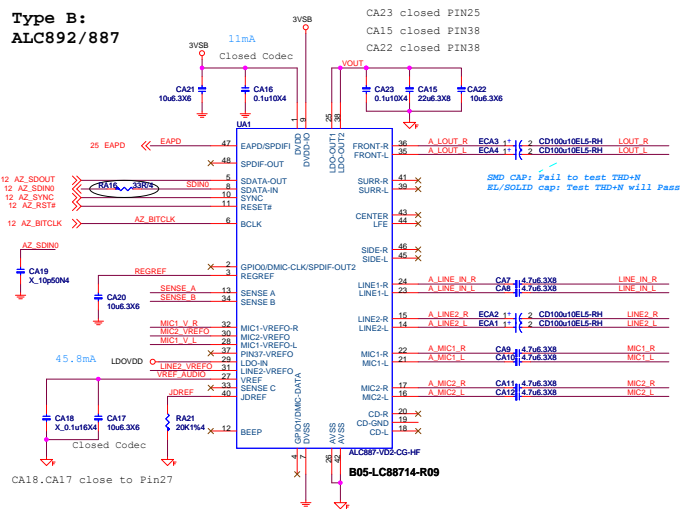
D03-0341409-A68 / D03-0230019-A30


## MS-7994 Add. Debug LED circuit



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7994</b>			
Size Custom	Document Description <b>BIOS ROM/TPM/Debug LED</b>		Rev 11
Date: Thursday, October 29, 2015		Sheet 23	of 54

Type B:  
ALC892/887

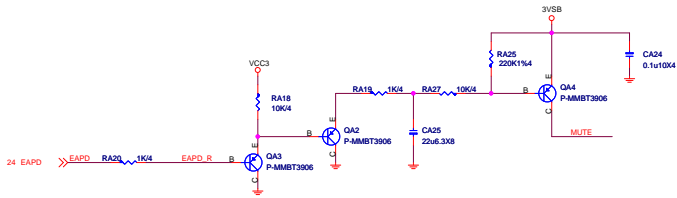


	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7994</b>		
	Size Custom	Document Description <b>AUDIO 887</b>	Rev 11
	Date: Thursday, October 29, 2015		Sheet 24 of 54



**Rear Line OUT De-POP circuit**

De-pop circuit for Rear Line out & Front Headphone out)



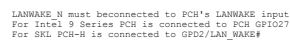
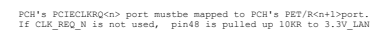
Digital

Analog



MICRO-STAR INT'L CO.,LTD		
MS-7994		
Doc Custom	Document Description AUDIO de-pop circuit	Rev 11
Date: Thursday, October 26, 2018 [Sheet 26 of 54]		

MS-7994 change to using I219

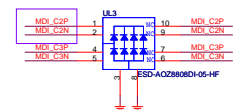
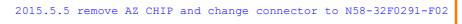


```

SMBUS PULL-UP OPTIONS
SMBUS SPEED
1MHz (Default setting)  499 ohm
100KHz/400KHz           2.2K ohm

```

Remove pull-up R if R existence on motherboard (or PCH has internal pull-up R).



Do not pair MDI0 and MDI1 on the same TVSdevice  
(avoid LAN POE connecting issue).  
Otherpairing combination is ok.

D0G-06A050C-A68  
D0G-05A0300-I14

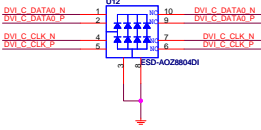


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7994</b>			
Size Custom	Document Description <b>LAN - Intel I219V</b>		Rev 11
Date: Thursday, October 29, 2015		Sheet 26 of 54	

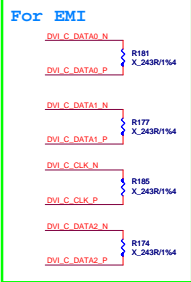
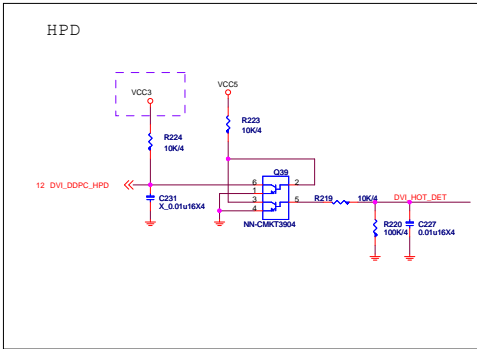
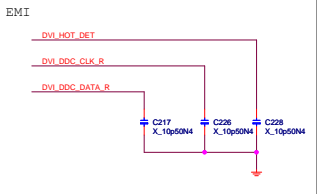
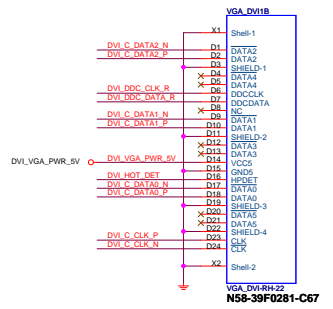
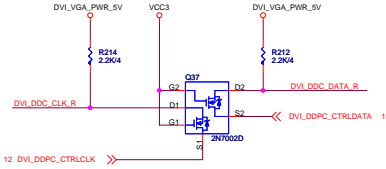
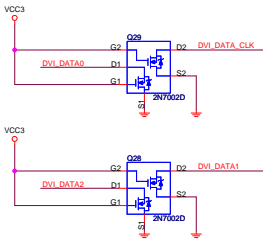
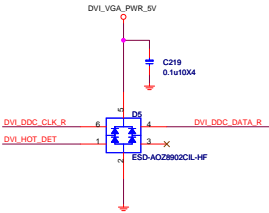
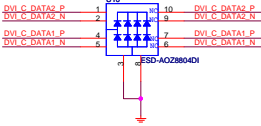
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



U12 AVL:D0G-05A050C-005  
D0G-06A050C-A68

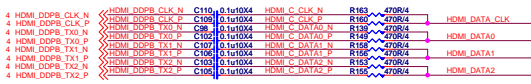


U10 AVL:D0G-05A050C-005  
D0G-06A050C-A68

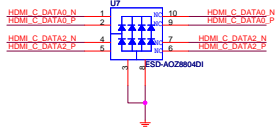


MICRO-STAR INT'L CO.,LTD			
MS-7994			
Size	Document Description	Rev	11
Custom	DVI Connector		
Date: Thursday, October 29, 2015		Sheet	27 of 54

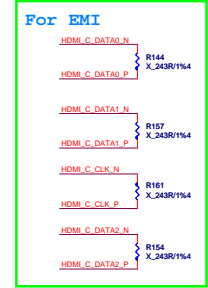
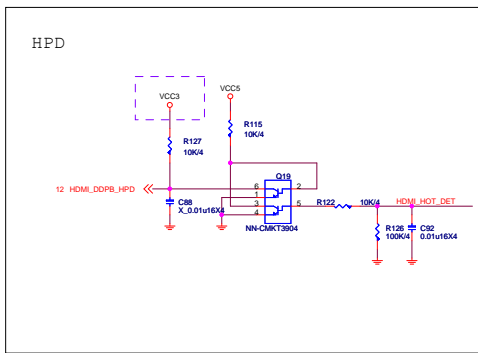
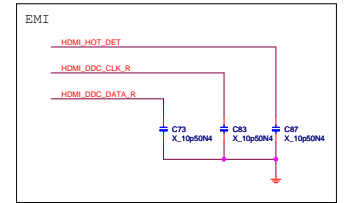
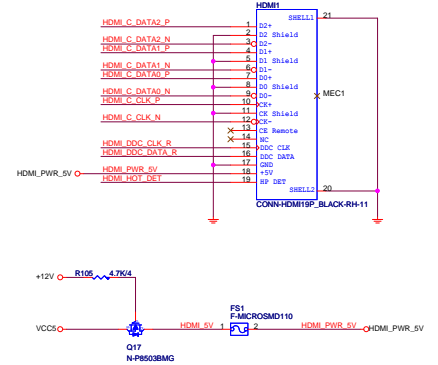
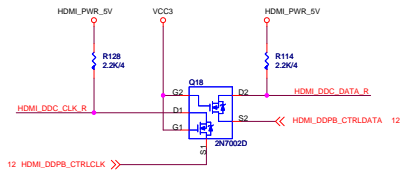
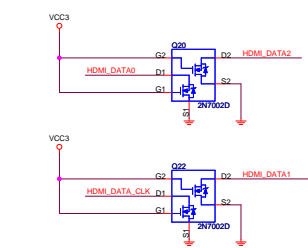
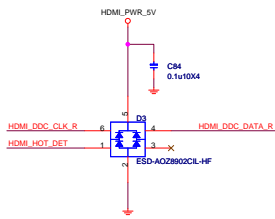
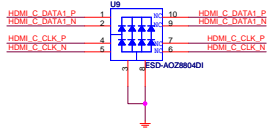
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68



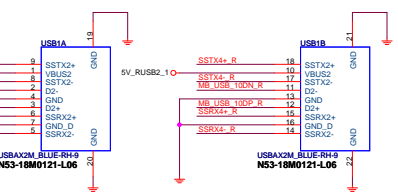
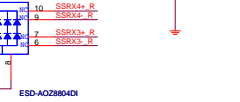
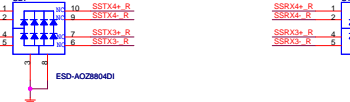
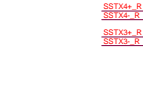
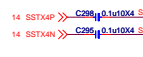
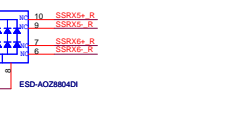
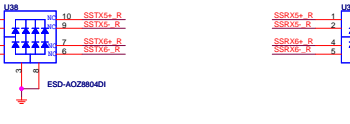
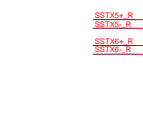
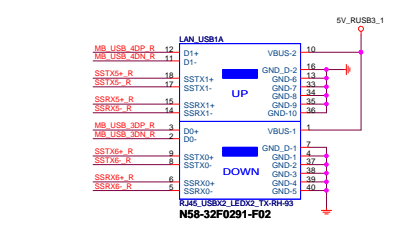
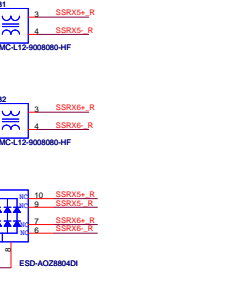
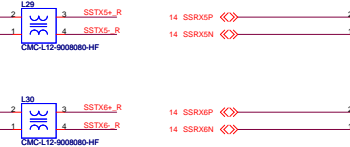
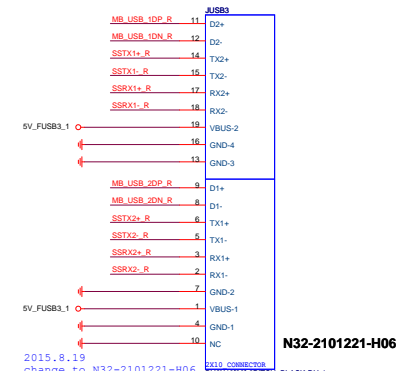
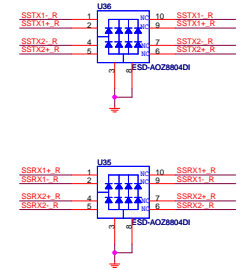
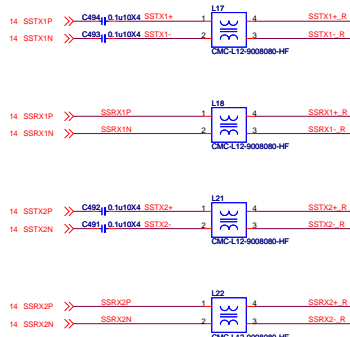
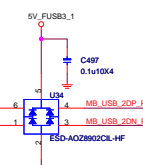
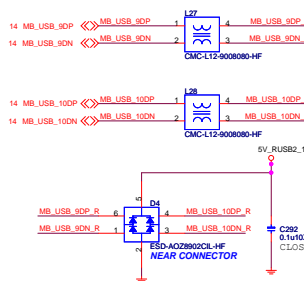
U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



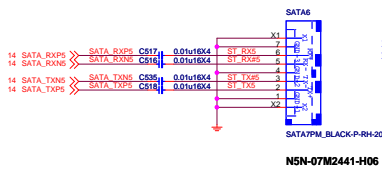
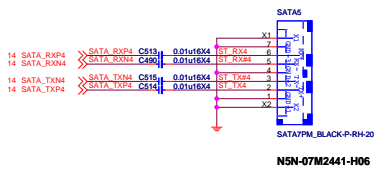
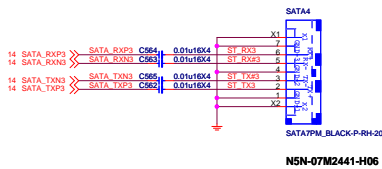
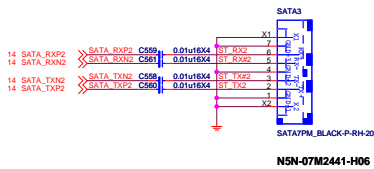
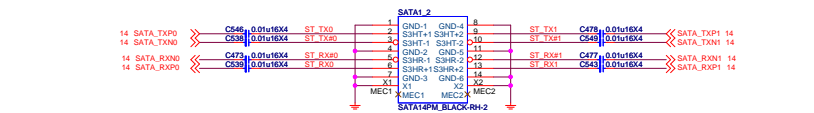
MICRO-STAR INT'L CO.,LTD		
MS-7994		
Size	Document Description	Rev
Custom	HDMI Connector	11
Date: Thursday, October 28, 2015		Sheet 28 of 54





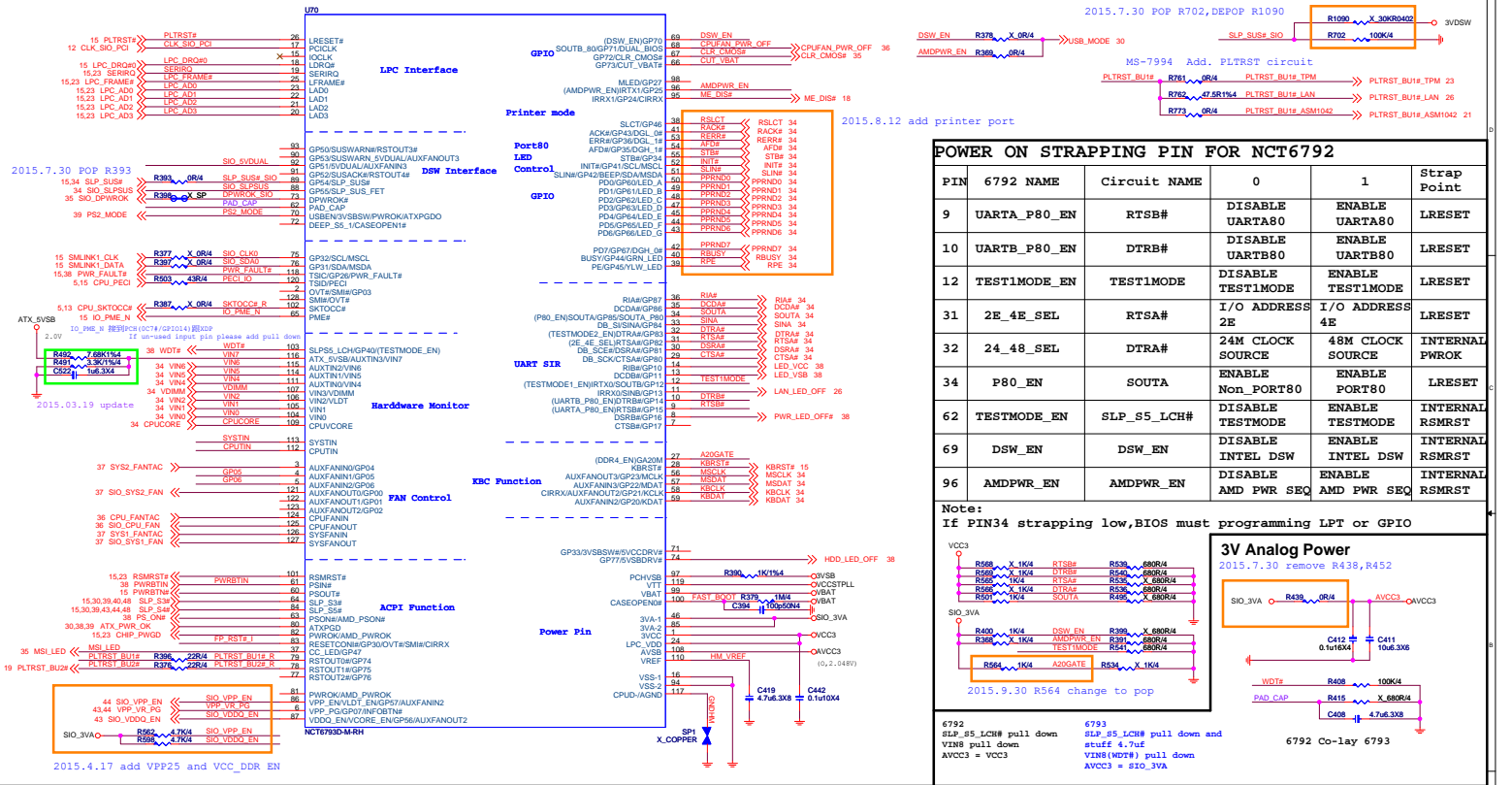


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7994</b>		
Size Custom	Document Description <b>USB3.0 Connector</b>	Rev 11
Date: Wednesday, October 26, 2011 15:00:00 24 24		



H110: SATA5 & SATA6 depop  
B150: SATA5 & SATA6 pop



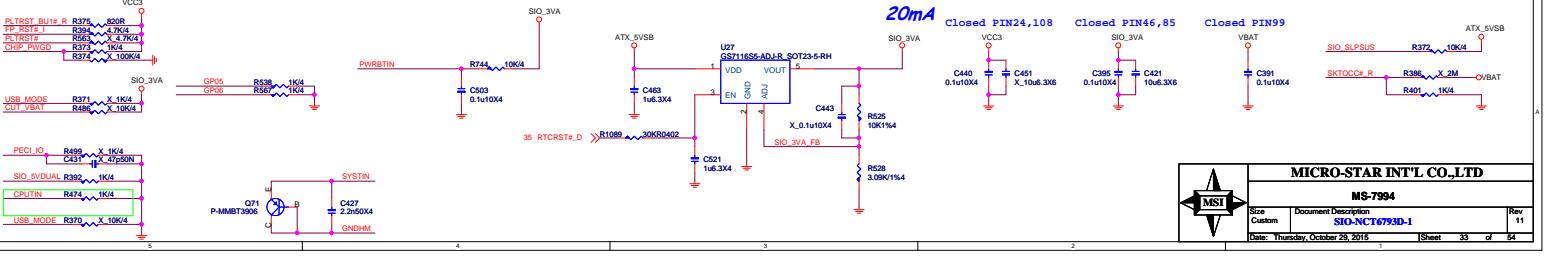


POWER ON STRAPPING PIN FOR NCT6792					
PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:  
If PIN34 strapping low, BIOS must programming LPT or GPIO

2015.7.30 remove R438, R452

3V Analog Power



**MICRO-STAR INT'L CO., LTD**  
**MS-7994**  
Size: Custom  
Document Description: SIO-NCT6793D-1  
Date: Thursday, October 29, 2015  
Sheet: 33 of 54

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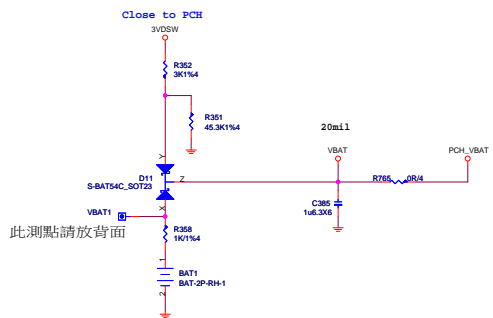
[illegible]

MS-7994

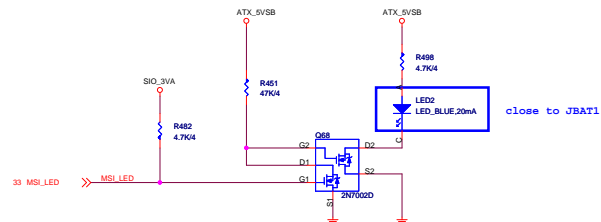
**SIO-NCT6793**

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2015.7.30 Update circuit

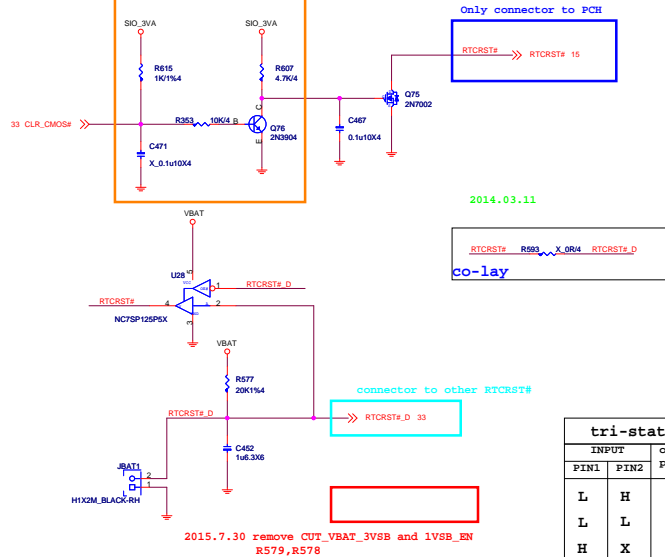


MSI\_LED



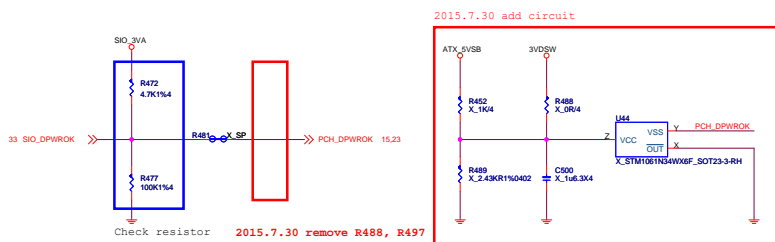
BIOS MODE

2015.4.24 update CLR\_COMS circuit

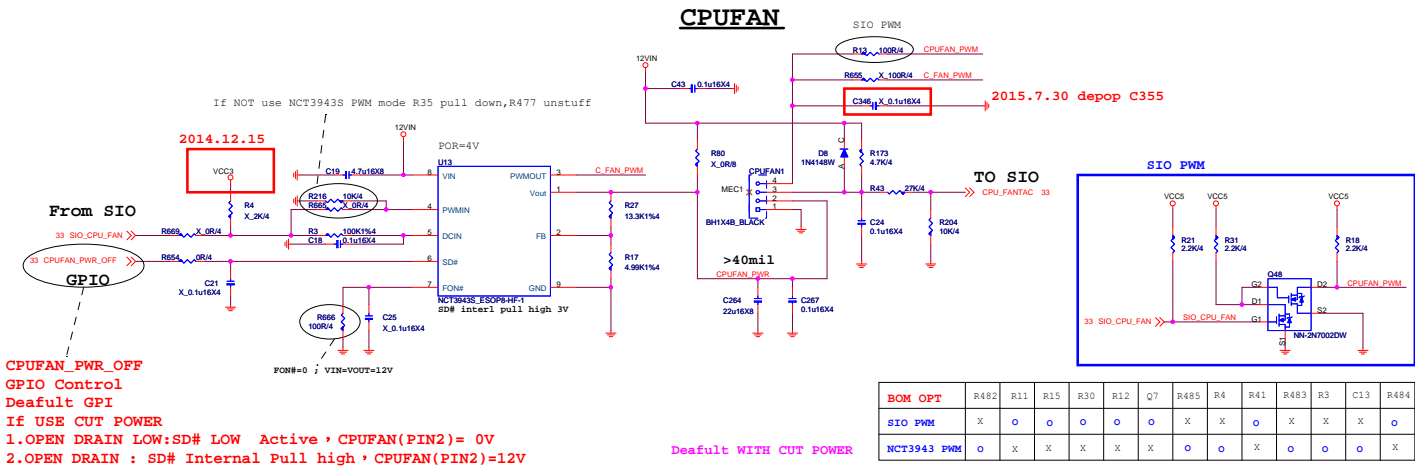


CUT 3VSB 2015.7.30 remove CUT\_3VSB circuit

CUT PCH\_1VSB 2015.7.30 remove CUT\_PCH\_1VSB circuit

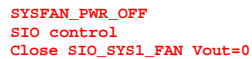


Type I : 4 PIN CPU FAN USE SIO PWM (STUFF NCT3943S WITH GPIO CUT POWER)

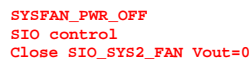


BOM OPT	R482	R11	R15	R30	R12	Q7	R485	R4	R41	R483	R3	C13	R484
SIO PWM	X	O	O	O	O	O	X	X	O	X	X	X	O
NCT3943 PWM	O	X	X	X	X	X	O	O	X	O	O	O	X

## MS-7994 SYS FAN is Type : H



MS-7994 SYS FAN is Type : H and Add. FAN control for SIO Pin3, 121



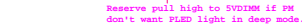
R289,Q52,R305 close to JPWR1



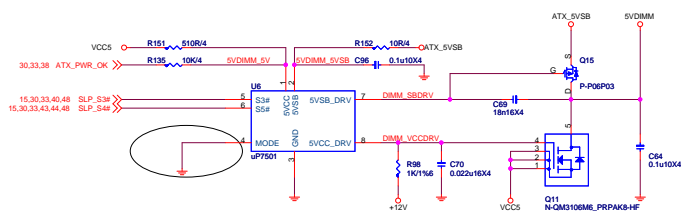
VCC5



SIO\_GP33 Default : GPI/VS#  
BIOS set it to GPI/PP/H  
NS Active : GPO/OD/L

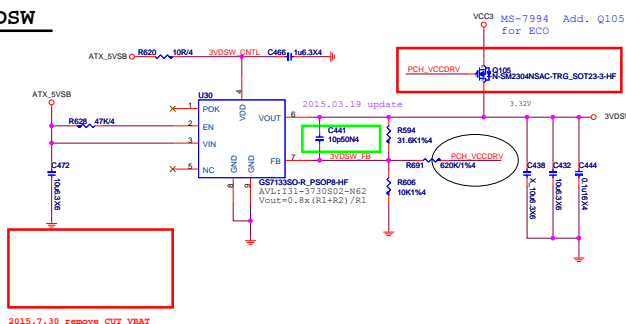


```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```



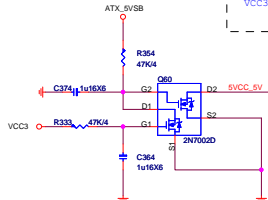
```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

## 1A

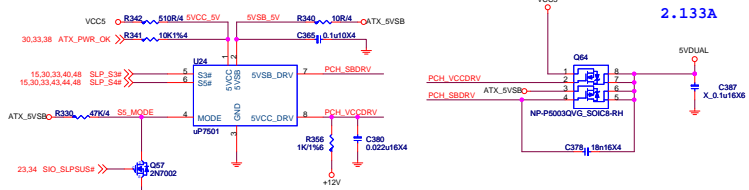


2015.7.30 remove CUT VBAT

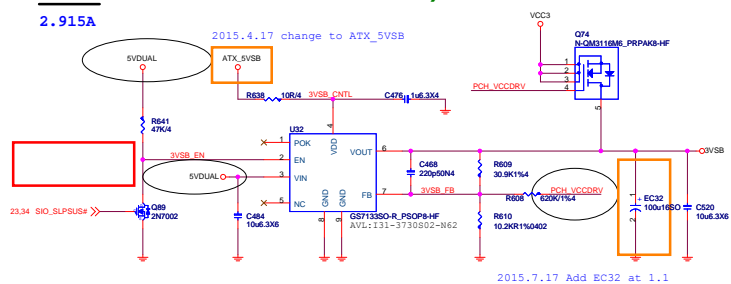
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



SVDUAL is power source of LPQSP



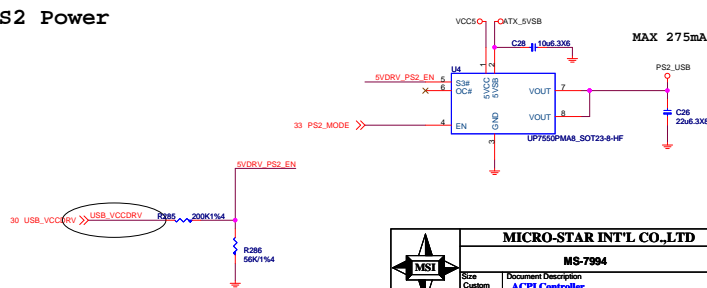
## 2.915A




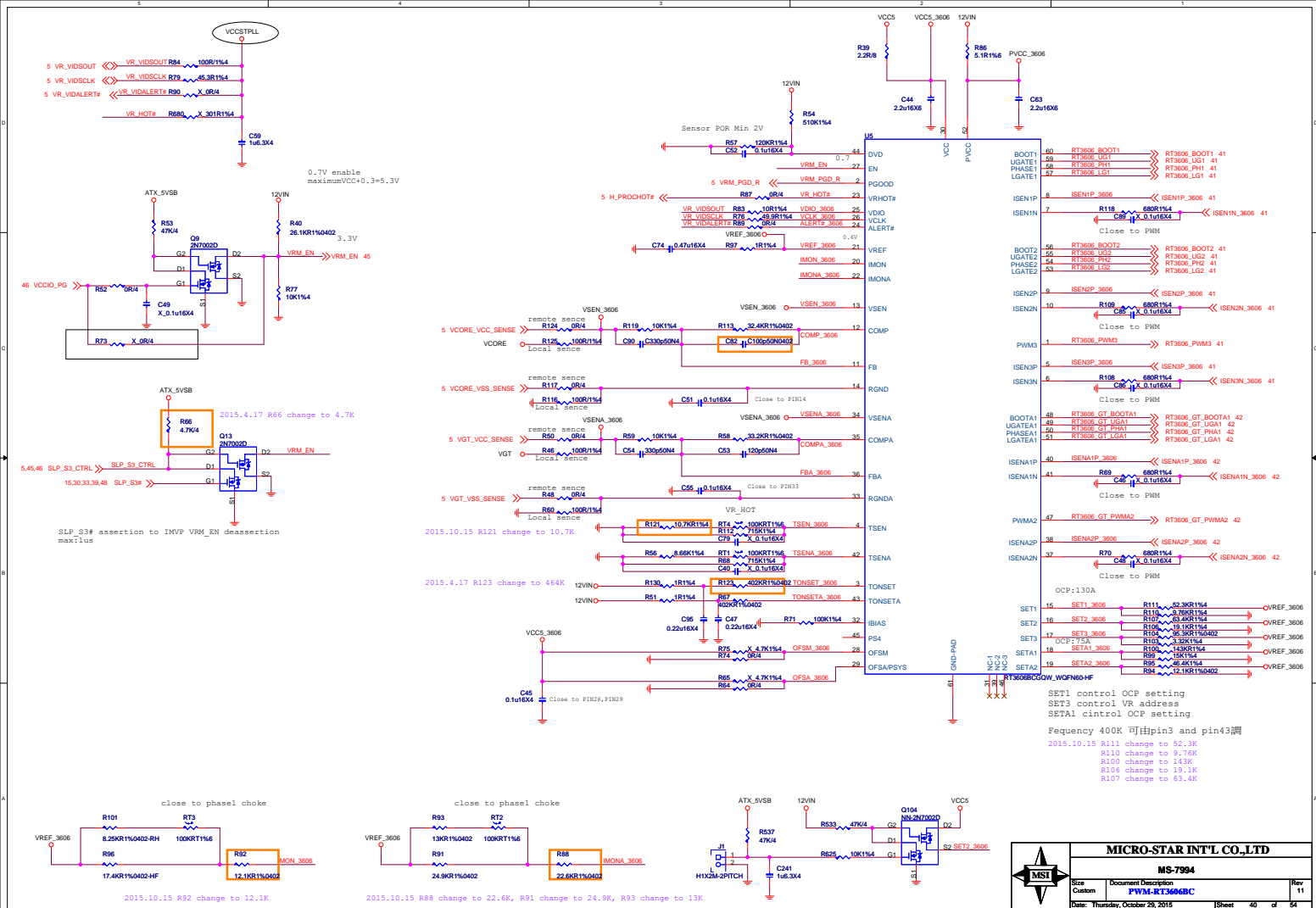
2015.7.30 remove CUT\_VBAT\_3VSE

```
VFB=3.224V for S0->S3 3VSB voltage raise & ATX 5VSB drop.
```

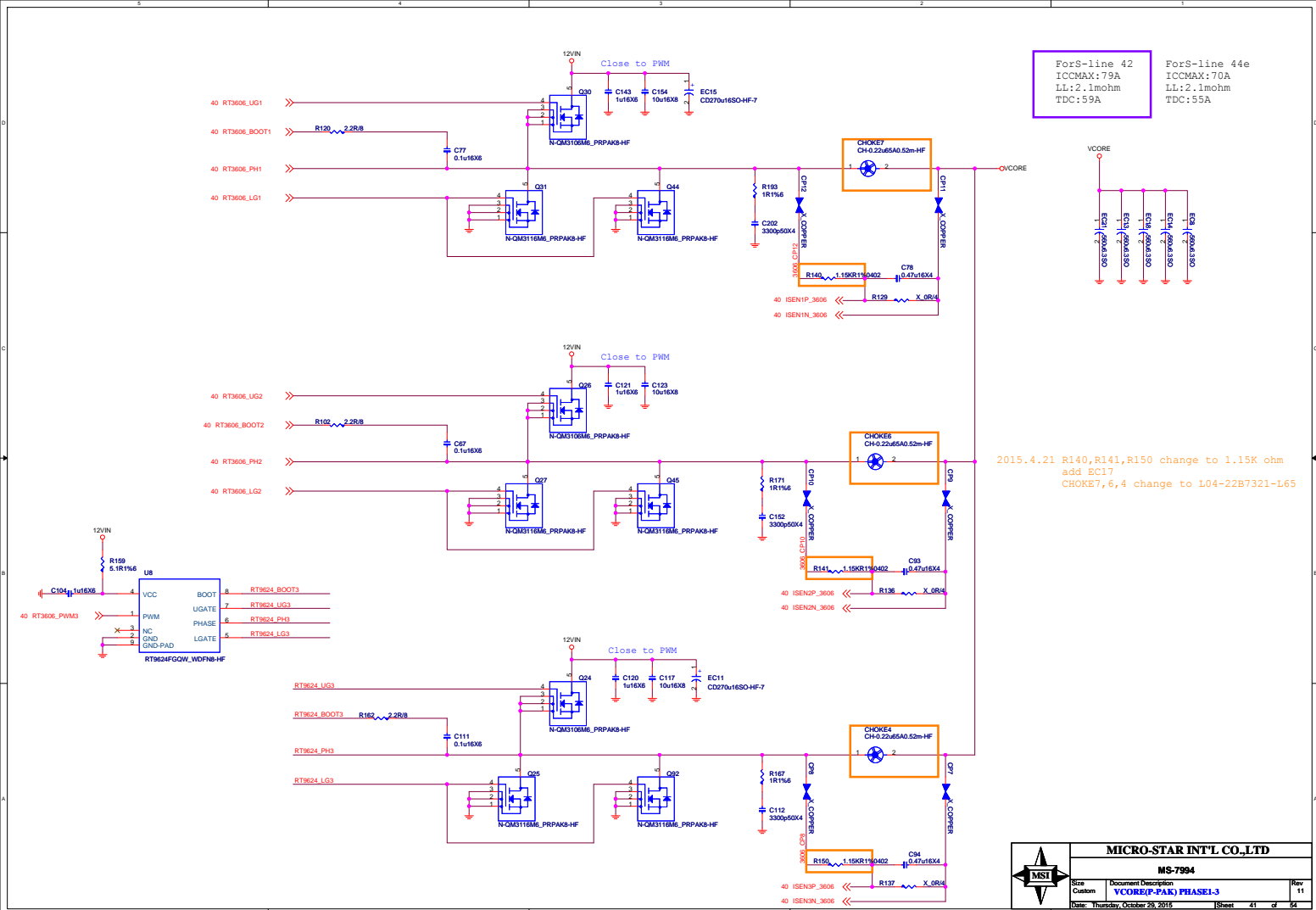
30 USB\_VCCDRV USB\_VCCDRV R085 200K1%4

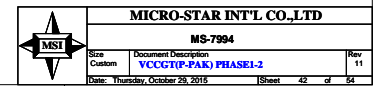


	<b>MICRO-STAR INT'L CO., LTD</b>		
	<b>MS-7994</b>		
	Size Custom	Document Description <b>ACPI Controller</b>	Rev 11
	Date: Thursday, October 26, 2014		1 Sheet 36 of 64





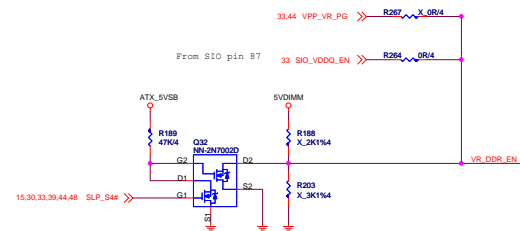
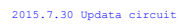




2.8A FOR CPU  
4.8A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

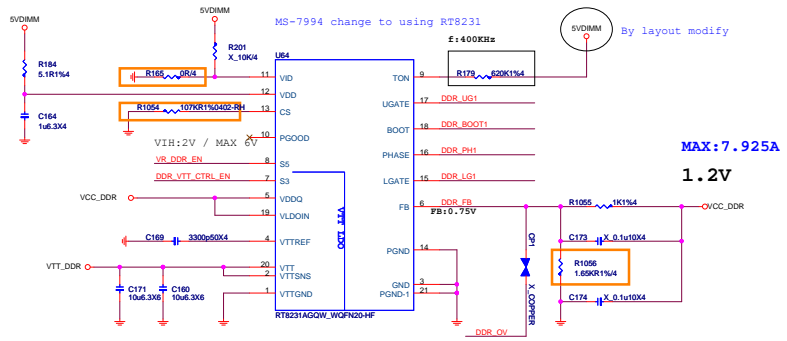
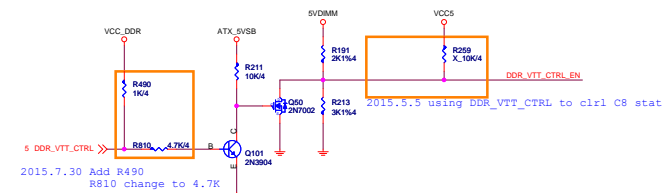
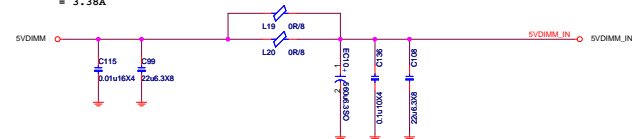
$$\text{Current limit} = 95.3K(R1054) * 5\mu A / 10 / 4\text{mohm} = 11.91A$$

VID	Reference Voltage (V)
H	0.675
L	0.75

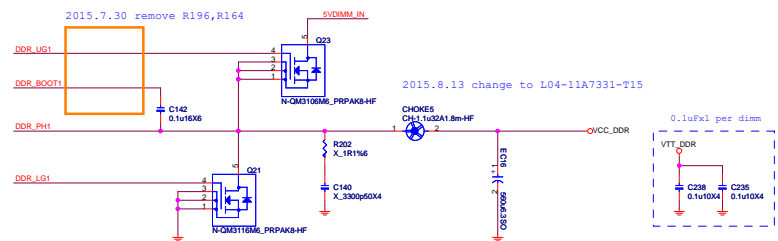


```
SLP_S4# de-assertion to VDDQ ramp down start
VPP ramp down after VDDQ ramp down
```

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 7.925 * 0.427 \\ &= 3.38A \end{aligned}$$



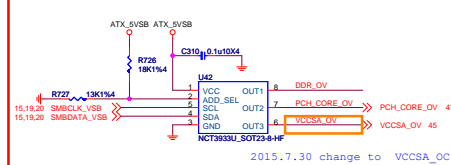
MAX:7.925A  
1.2V



0x26:RH=18K,RL=13K

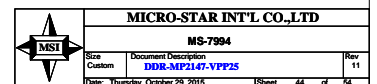
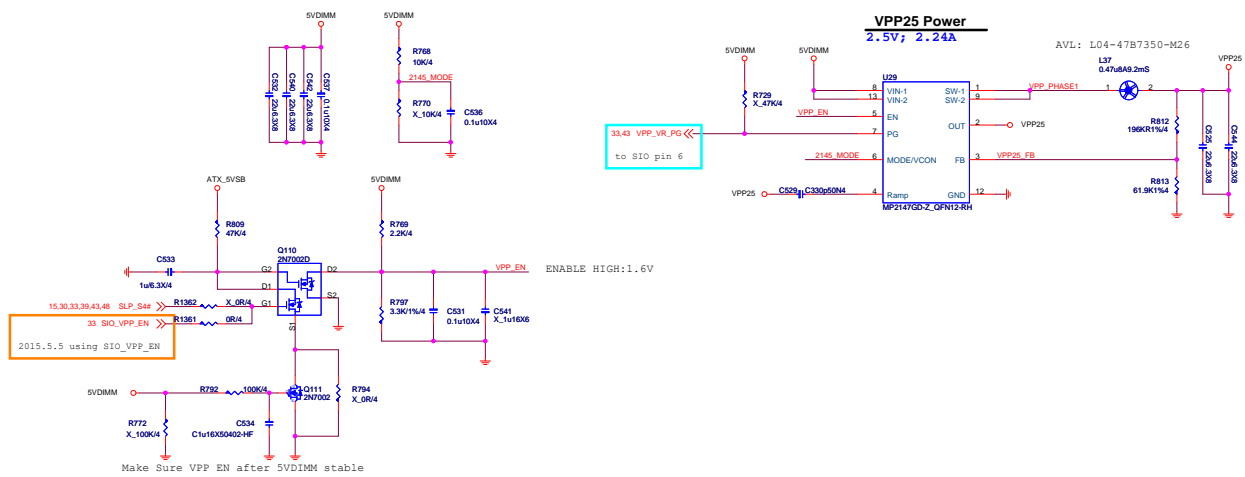
0x26:RH=18K,RL=13K

step-down function



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7994</b>			
Size Custom	Document Description <b>DDR-R78231</b>		Rev 11
Date: Thursday, October 29, 2015		Sheet 43 of	54

2DIMM :1.12A FOR DDR VPP2.5V



# SA Power:1.05V,12.3A

OCp =12.3A\*1.4=17.22A

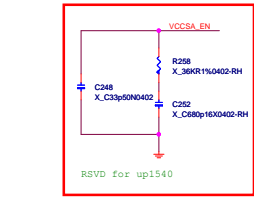
Rocs(R15)=OCp\*Rdson(Low side)3.4mohm/10uA

=17.22\*(2.5)mohm/10uA

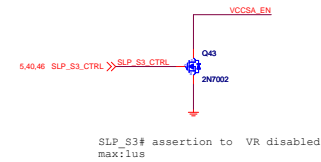
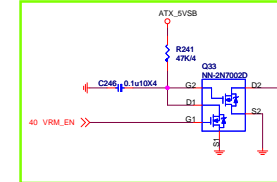
=4.305Kohm

Rocs=5.76K,OCp:  
D03-4C05N03-O05 : 16.94A  
D03-632BA0C-N03 : 17.45A  
use UBIQ MOS need Check

Rdson(Low)10V  
D03-4C05N03-O05 : 3.4mohm  
D03-632BA0C-N03 : 3.3mohm  
D03-3056M00-U47 : 4.2mohm



2015.7.30 Update circuit

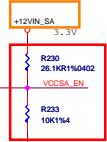


2014.12.25  
for up1540:C242,R234 ->NC  
for RT8125: C242:1000p,R234->768R

2014.12.25  
for up1540:R1039 is OCP set min:5K ohm  
stuff 5.36K OCP SET:15.76A  
for RT8125:R1039->1000p

2015.01.22  
for up1540:stuff R258->36K,  
C248->33p,C252->680p  
for RT8125:R258,C248,C252->NC

2015.9.30  
change to +12VIN\_SA



2014.12.25  
for up1540:R230,R122 ->NC

2015.01.22  
for up1540:R1->2.2R  
for RT8125:R1->10R

2015.8.11  
U14 change to RT8125E I32-8125E0C-R11

2015.4.17  
for up1540:R764->OR  
for RT8125:R764->NC

2015.4.17  
for up1540:R814->OR  
for RT8125:R814->OR

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

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for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

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for up1540:R236 change to 3.24K

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for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

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for up1540:R236 change to 3.24K

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for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

2015.4.17  
for up1540:R236 change to 3.24K

$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$
$$= 12.3 * 0.2825$$
$$= 2.64A$$

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$
$$= 0.5193uH (K = 30\%)$$



MICRO-STAR INT'L CO.,LTD		
MS-7994		
Doc	Document Description	Rev
Custom	VCCSA POWER-RT8125	11
Date: Thursday, October 29, 2015		Sheet 45 of 54

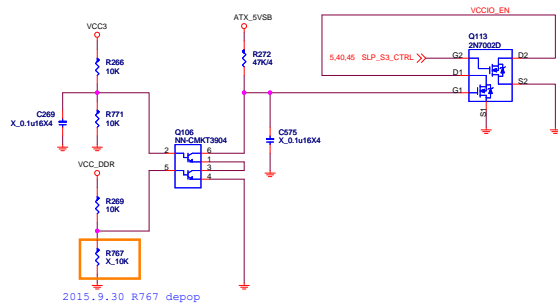
0.95V; 5.5A

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

$$0.7776\mu H < L < 1.1664\mu H$$

```
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off. <500ms
```

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



## 2015.8.11 remove OV circuit



MS-7994

Size Custom	Document Description <b>VCCIO POWER-NB681</b>	Rev 11
Date: Thursday, October 29, 2015		Sheet 46 of 54

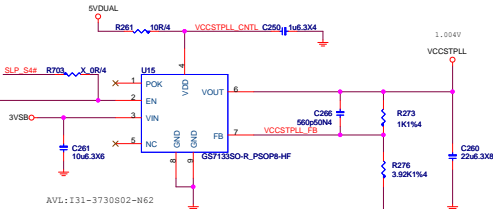
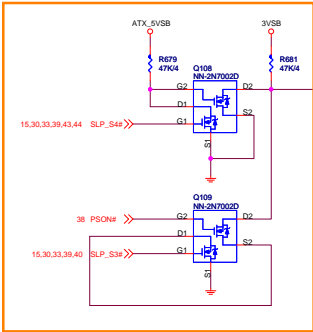


VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO  
and H110



2015.8.11 remove circuit R560

VCCIO ramped and stable before  
beginning of VCCOPC/VCCOPPIO ramp  
VCCST/PLL stable 1ms before PROCFWGRD

PCH\_1P8

2015.8.25 remove circuit

1.8V; 53mA for PCH-H VCCPGPPA

VCCPLL\_OC


2015.8.7 remove circuit

1.2V; 100mA



MICRO-STAR INT'L CO.,LTD		
MS-7994		
Doc Custom	Document Description VCCSTPLL	Rev 11
Date: Thursday, October 29, 2015		Sheet 48 of 54





MICRO-STAR INT'L CO.,LTD		
MS-7994		
Size	Document Description	Rev
Custom	NA	11
Date: Thursday, October 29, 2015		Sheet 49 of 54

